



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/742,386	12/22/2000	Norio Kimura	2000-1761A	8728

513 7590 03/28/2005

WENDEROTH, LIND & PONACK, L.L.P.  
2033 K STREET N. W.  
SUITE 800  
WASHINGTON, DC 20006-1021

EXAMINER

MOORE, KARLA A

ART UNIT	PAPER NUMBER
----------	--------------

1763

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/742,386

**Applicant(s)**

KIMURA ET AL.

**Examiner**

Karla Moore

**Art Unit**

1763

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 December 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-72 is/are pending in the application.
- 4a) Of the above claim(s) 46-61 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-45 and 62-72 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 December 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 0701,1201.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Election/Restrictions*

1. Claims 60-61 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 12/30/04. Claims 46-59 of the application were withdrawn previously.
2. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless —(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 27, 31, 65-66, 68-70 and 72 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,267,853 to Dordi et al. (1).**
5. Dordi et al. (1) disclose a semiconductor substrate processing apparatus in Figure 3, comprising: a carry-in and carry-out section (210; column 5, rows 20) for carrying in and carrying out a semiconductor substrate having a surface on which a circuit is formed, the apparatus is capable of carrying in and out in a dry state by using spin/rinse/dry station (212; column 5, row 24); a plated metal/electroplating film forming unit (240; column 5, rows 41-46) for forming a plated metal film on said semiconductor substrate

Art Unit: 1763

which has been carried in; a bevel etching unit (one of modules 236; column 9, rows 1-6 and column 19, rows 5-10 and 48-50) for etching a peripheral edge portion of said semiconductor substrate; and a transport mechanism (216) for transporting said semiconductor substrate between said units. The processing apparatus of Dordi et al. (1) may further comprise an annealing unit (211; column 5, row 20) for annealing said semiconductor substrate. The processing apparatus of Dordi et al. (1) may further comprise a cleaning and drying unit for cleaning and drying said semiconductor substrate (one of modules 238; column 9, rows 1-6 and column 19, rows 5-10) and electroless plating cells (215; column 12, rows 20-21) capable of forming a seed layer on said semiconductor substrate or reinforcing a seed layer on a substrate. Further, one of the electroplating units (240) could be used as a cover plating unit for forming a plated cover layer on said semiconductor substrate. The apparatus also comprises a liquid supply equipment having a liquid plating tank (220, column 20, rows 51-59).

6. With respect to claim 31, treatment in said plated film forming unit is performed with said semiconductor held by a substrate holding portion (Figure 6, 450; column 5, rows 45-47).

7. Additionally, with respect to claim 69 and the process(es) performed in the plated metal film forming unit, depending on the processing material supplied (column 21, rows 7-20) any number of processes could be performed. The courts have ruled that a claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). The courts have further ruled that expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim. Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969).

#### ***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 1763

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. **Claims 1-4, 7-18, 36, 44, 62 and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,267,853 to Dordi et al. (1) in view of U.S. Patent No. 6,309,981 to Mayer et al.**

11. Dordi et al. (1) disclose the invention substantially as claimed in Figure 3 and comprising: a semiconductor substrate processing apparatus, comprising: a carry-in and carry-out section (210; column 5, rows 20) for carrying in and carrying out a semiconductor substrate having a surface on which a circuit is formed, the apparatus is capable of carrying in and out in a dry state by using spin/rinse/dry station (212; column 5, row 24); a plated metal film forming unit (240; column 5, rows 41-46) for forming a plated metal film on said semiconductor substrate which has been carried in; a bevel etching unit (one of modules 236; column 9, rows 1-6 and column 19, rows 5-10 and 48-50) for etching a peripheral edge portion of said semiconductor substrate; and a transport mechanism (216) for transporting said semiconductor substrate between said units.

12. However, Dordi et al. (1) fail to disclose the apparatus comprising a polishing unit for polishing at least part of said plated metal film on said semiconductor substrate.

13. Mayer et al. disclose using a polishing process after a plated metal film forming process and an edge bevel removal process in a semiconductor manufacturing process for the purpose of planarizing a substrate for further processing (column 5, rows 56-61).

Art Unit: 1763

14. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided a polishing apparatus for use after plating and edge bevel removal processes in Dordi et al. (1) in order to planarize a substrate for further processing as taught by Mayer.

15. With respect to claim 2, the processing apparatus of Dordi et al. (1) may further comprise a cleaning unit for cleaning said semiconductor substrate (one of modules 238; column 9, rows 1-6 and column 19, rows 5-10).

16. With respect to claim 3, the processing apparatus of Dordi et al. (1) may further comprise an annealing unit (211; column 5, row 20) for annealing said semiconductor substrate.

17. With respect to claim 4, said plated metal film forming unit comprises an electroplating unit (column 5, rows 41-46).

18. With respect to claims 7-10, the processing apparatus may further comprise electroless plating cells (215; column 12, rows 20-21) capable of forming a seed layer on said semiconductor substrate or reinforcing a seed layer on a substrate.

19. With respect to claim 11, one of the electroplating units (240) could be used as a reinforcing seed layer forming unit.

20. With respect to claims 12 and 67, Dordi et al. (1) further fail to teach a barrier layer forming unit for forming a barrier layer on said semiconductor substrate.

21. Mayer et al. teach the use of a barrier layer forming process in a semiconductor manufacturing process for the purpose of protecting underlying silicon devices from the diffusion of metal ions (column 5, rows 5-24).

22. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided a barrier layer forming unit in Dordi et al. (1) in order to form a barrier layer during a semiconductor manufacturing process so that an underlying silicon device could be protected from the diffusion of metal ions as taught by Mayer et al.

Art Unit: 1763

23. With respect to claim 13, one of the electroplating units (240) could be used as a cover plating unit for forming a plated cover layer on said semiconductor substrate.

24. With respect to the language of claims 14-18 that recite duplication of a polishing apparatus, the courts have ruled that the mere duplication of parts has no patentable significance unless a new and unexpected result is produced. In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). With respect to the language of claims 14-18 that is drawn to intended uses of the duplicate apparatus the courts have ruled that a claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). Finally with respect to the language of claims 14-18 that refers to the article worked upon in the polishing units the courts have ruled that the inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims. In re Young, 75 F.2d 966, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 312 F.2d 937, 136 USPQ 458, 459 (CCPA 1963)).

25. With respect to claim 36, Dordi et al. (1) disclose the invention substantially as claimed in Figure 3 and comprising: a semiconductor substrate processing apparatus, comprising: a carry-in and carry-out section (210; column 5, rows 20) for carrying in and carrying out a semiconductor substrate having a surface on which a circuit is formed, the apparatus is capable of carrying in and out in a dry state by using spin/rinse/dry station (212; column 5, row 24); a plated metal film forming unit (240; column 5, rows 41-46) for forming a plated metal film on said semiconductor substrate which has been carried in; and a transport mechanism (216) for transporting said semiconductor substrate between said units. Treatment in said plated film forming unit is performed with said semiconductor held by a substrate holding portion (Figure 6, 450; column 5, rows 45-47).

26. However, Dordi et al. (1) fail to disclose the apparatus comprising a polishing unit for polishing at least part of said plated metal film on said semiconductor substrate.

Art Unit: 1763

27. Mayer et al. disclose using a polishing process after a plated metal film forming process and an edge bevel removal process in a semiconductor manufacturing process for the purpose of planarizing a substrate for further processing (column 5, rows 56-61).

28. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided a polishing apparatus for use after a plating process in Dordi et al. (1) in order to planarize a substrate for further processing as taught by Mayer. With respect to the different types of treatments performed in the plating metal film forming unit, the courts have ruled that a claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987).

29. With respect to claim 44, Dordi et al. (1) disclose the invention substantially as claimed in Figure 3 and comprising: a semiconductor substrate processing apparatus, comprising: a carry-in and carry-out section (210; column 5, rows 20) for carrying in and carrying out a semiconductor substrate having a surface on which a circuit is formed, the apparatus is capable of carrying in and out in a dry state by using spin/rinse/dry station (212; column 5, row 24); a plated metal film forming unit (240; column 5, rows 41-46) for forming a plated metal film on said semiconductor substrate which has been carried in;; and a transport mechanism (216) for transporting said semiconductor substrate between said units. With respect to the process(es) performed in the plated metal film forming unit, depending on the processing material supplied (column 21, rows 7-20) any number of processes could be performed. The courts have ruled that a claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). The courts have further ruled that expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim. Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969).



Art Unit: 1763

30. However, Dordi et al. (1) fail to disclose the apparatus comprising a polishing unit for polishing at least part of said plated metal film on said semiconductor substrate.

31. Mayer et al. disclose using a polishing process after a plated metal film forming process and an edge bevel removal process in a semiconductor manufacturing process for the purpose of planarizing a substrate for further processing (column 5, rows 56-61).

32. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided a polishing apparatus for use after plating and edge bevel removal processes in Dordi et al. (1) in order to planarize a substrate for further processing as taught by Mayer.

33. With respect to claim 62, Dordi et al. (1) and Mayer et al. disclose the apparatus as claimed, which is thoroughly described above.

**34. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dordi et al. (1) and Mayer et al. as applied to claims 1-4, 7-18, 36, 44, 62 and 67 above, and further in view of U.S. Patent No. 5,310,410 to Begin et al**

35. Dordi et al. (1) and Mayer et al. disclose the invention substantially as claimed and as described above.

36. However, Dordi et al. (1) and Mayer et al. fail to teach the apparatus may further comprise a film thickness measuring instrument and/or a detection sensor for measuring and/or detecting a film thickness of a film and/or surface state of a film formed on said semiconductor substrate.

37. Begin et al. teach that an inspection unit may be included as part of a cluster apparatus for the purpose of determining whether a substrate or a portion of the apparatus is defective (column 4, rows 48-54).

38. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided an inspection unit in Dordi et al. (1) and Mayer et al. in order to determine whether a substrate or a portion of the apparatus is defective as taught by Begin et al.

Art Unit: 1763

39. Additionally, with respect to claim 6, which is drawn to an order of processing during an intended use of the apparatus, the courts have ruled that a claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987).

40. **Claims 19-21, 23-26 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,267,853 to Dordi et al. (1) in view of U.S. Patent No. 6,309,981 to Mayer et al. and U.S. Patent No. 5,083,364 to Olbrich et al.**

41. Dordi et al. (1) disclose the invention substantially as claimed in Figure 3 and comprising: a semiconductor substrate processing apparatus, comprising: a carry-in and carry-out section (210; column 5, rows 20) for carrying in and carrying out a semiconductor substrate having a surface on which a circuit is formed, the apparatus is capable of carrying in and out in a dry state by using spin/rinse/dry station (212; column 5, row 24); a plated metal film forming unit (240; column 5, rows 41-46) for forming a plated metal film on said semiconductor substrate which has been carried in; a bevel etching unit (one of modules 236; column 9, rows 1-6 and column 19, rows 5-10 and 48-50) for etching a peripheral edge portion of said semiconductor substrate; and a transport mechanism (216) for transporting said semiconductor substrate between said units.

42. However, Dordi et al. (1) fail to disclose the apparatus comprising a polishing unit for polishing at least part of said plated metal film on said semiconductor substrate.

43. Mayer et al. disclose using a polishing process after a plated metal film forming process and an edge bevel removal process in a semiconductor manufacturing process for the purpose of planarizing a substrate for further processing (column 5, rows 56-61).

44. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided a polishing apparatus for use after plating and edge bevel removal processes in Dordi et al. (1) in order to planarize a substrate for further processing as taught by Mayer.

Art Unit: 1763

45. Dordi et al. (1) and Mayer et al. disclose the invention substantially as claimed and as described above.

46. However, Dordi et al. (1) and Mayer et al. fail to disclose any of the processing units a interchangeable.

47. Olbrich et al. disclose a multi-chamber semiconductor manufacturing apparatus with interchangeable process module for the purpose of connection modules depending on purpose, thus allowing for assembly and modification of the apparatus to meet various needs which leads to increased productivity while reducing the proportionate expense (column 1, rows 27-33 and 46-57).

48. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided interchangeable modules in Dordi et al. (1) and Mayer et al. in order to connect modules depending on purpose, thus allowing for assembly and modification of the apparatus to meet various needs which leads to increased productivity while reducing the proportionate expense as taught by Olbrich et al.

49. Examiner notes that based on the motivation of Olbrich et al. for providing interchangeable units, it would have been obvious to interchange any of the units on the apparatus.

50. With respect to claims 20-21, 23-24 and 26, the apparatus may further comprise a cleaning unit (one of modules 238; column 9, rows 1-6 and column 19, rows 5-10), an annealing unit (211; column 5, row 20), and a reinforcing seed layer forming unit/seed layer forming unit (215; column 12, rows 20-21), and a cover layer plating unit (240) all of which would be interchangeable, based on the motivation provided by Olbrich et al. described above.

51. With respect to claim 25, Dordi et al. (1) fails to teach a barrier layer forming unit for forming a barrier layer on said semiconductor substrate.

52. Mayer et al. teach the use of a barrier layer forming process in a semiconductor manufacturing process for the purpose of protecting underlying silicon devices from the diffusion of metal ions (column 5, rows 5-24).

Art Unit: 1763

53. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided a barrier layer forming unit in Dordi et al. (1) in order to form a barrier layer during a semiconductor manufacturing process so that an underlying silicon device could be protected from the diffusion of metal ions as taught by Mayer et al.

54. As noted above, based on the motivation of Olbrich et al. for providing interchangeable units, it would have been obvious to interchange any of the units on the apparatus.

55. With respect to claim 45, in addition to the units mentioned above, the processing apparatus of Dordi et al. (1) may further comprise a cleaning unit for cleaning said semiconductor substrate (one of modules 238; column 9, rows 1-6 and column 19, rows 5-10); an annealing unit (211; column 5, row 20) for annealing said semiconductor substrate; electroless plating cells (215; column 12, rows 20-21) capable of forming a seed layer on said semiconductor substrate or reinforcing a seed layer on a substrate; and a cover plating unit for forming a plated cover layer on said semiconductor substrate. Again, Examiner notes that based on the motivation of Olbrich et al. for providing interchangeable units, it would have been obvious to interchange any of the units on the apparatus.

**56. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dordi et al. (1), Mayer et al. and Olbrich et al. as applied to claims 19-21, 23-26 and 45 above, and further in view of U.S. Patent No. 5,310,410 to Begin et al**

57. Dordi et al. (1), Mayer et al. and Olbrich et al. disclose the invention substantially as claimed and as described above.

58. However, Dordi et al. (1), Mayer et al. and Olbrich et al. fail to teach the apparatus may further comprise a film thickness measuring instrument and/or a detection sensor for measuring and/or detecting a film thickness of a film and/or surface state of a film formed on said semiconductor substrate.

59. Begin et al. teach that an inspection unit may be included as part of a cluster apparatus for the purpose of determining whether a substrate or a portion of the apparatus is defective (column 4, rows 48-54).

Art Unit: 1763

60. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided an inspection unit in Dordi et al. (1), Mayer et al. and Olbrich et al. in order to determine whether a substrate or a portion of the apparatus is defective as taught by Begin et al.

61. As noted above, based on the motivation of Olbrich et al. for providing interchangeable units, it would have been obvious to interchange any of the units on the apparatus.

**62. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dordi et al. (1) as applied to claims 27, 31, 65-66, 68-70 and 72 above, in view of U.S. Patent No. 5,083,364 to Olbrich et al.**

63. Dordi et al. (1) disclose the invention substantially as claimed and as described above.

64. However, Dordi et al. (1) fail to disclose said plated metal film forming unit, said bevel etching unit and said annealing unit are interchangeable.

65. Olbrich et al. disclose a multi-chamber semiconductor manufacturing apparatus with interchangeable process module for the purpose of connection modules depending on purpose, thus allowing for assembly and modification of the apparatus to meet various needs which leads to increased productivity while reducing the proportionate expense (column 1, rows 27-33 and 46-57).

66. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided interchangeable modules in Dordi et al. (1) in order to connect modules depending on purpose, thus allowing for assembly and modification of the apparatus to meet various needs which leads to increased productivity while reducing the proportionate expense as taught by Olbrich et al.

**67. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dordi et al. (1) as applied to claims 27, 31, 65-66, 68-70 and 72 above, in view of U.S. Patent No. 5,310,410 to Begin et al. and U.S. Patent No. 5,083,364 to Olbrich et al.**

68. Dordi et al. (1) disclose the invention substantially as claimed and as described above.

Art Unit: 1763

69. However, Dordi et al. (1) fail to teach the apparatus may further comprise a film thickness measuring instrument and/or a detection sensor for measuring and/or detecting a film thickness of a film and/or surface state of a film formed on said semiconductor substrate.

70. Begin et al. teach that an inspection unit may be included as part of a cluster apparatus for the purpose of determining whether a substrate or a portion of the apparatus is defective (column 4, rows 48-54).

71. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided an inspection unit in Dordi et al. (1) in order to determine whether a substrate or a portion of the apparatus is defective as taught by Begin et al.

72. Dordi et al. (1) and Begin et al. disclose the invention substantially as claimed and as described above.

73. However, Dordi et al. (1) and Begin et al. fail to teach the processing units are interchangeable.

74. Olbrich et al. disclose a multi-chamber semiconductor manufacturing apparatus with interchangeable process module for the purpose of connection modules depending on purpose, thus allowing for assembly and modification of the apparatus to meet various needs which leads to increased productivity while reducing the proportionate expense (column 1, rows 27-33 and 46-57).

75. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided interchangeable modules in Dordi et al. (1) and Begin et al. in order to connect modules depending on purpose, thus allowing for assembly and modification of the apparatus to meet various needs which leads to increased productivity while reducing the proportionate expense as taught by Olbrich et al.

76. **Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dordi et al. (1), Begin et al. and Olbrich et al. as applied to claim 29 above, and further in view of U.S. Patent No. 6,084,419 to Sato et al.**

77. Dordi et al. (1), Begin et al. and Olbrich et al. disclose the invention substantially as claimed and as described above.

Art Unit: 1763

78. However, over Dordi et al. (1), Begin et al. and Olbrich et al. fail to teach said film thickness measuring unit may have an alignment function for said semiconductor substrate.

79. Sato et al. disclose the use of an alignment function for use with an inspection unit (e.g film thickness measuring unit) for the purpose of aligning a substrate with the inspection probes (column 1, rows 26-37).

80. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided the film thickness measuring unit in Dordi et al. (1), Begin et al. and Olbrich et al. in order to align a substrate with the inspection probes as taught by Sato et al.

**81. Claims 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dordi et al. (1) as applied to claims 27, 31, 65-66, 68-70 and 72 above, in view of U.S. Patent Publication No. 2002/0157960 A1 to Dordi et al. (2).**

82. Dordi et al. (1) disclose the invention substantially as claimed and as described above.

83. However, Dordi et al. (1) fail to teach said plated film forming unit comprises a substrate holding portion for holding said semiconductor substrate such that a surface to be plated faces upward, an anode disposed above a surface to be plated, a cathode electrode for passing an electric current in contact with said substrate, and performs plating using a plating liquid in a space formed between said surface to be plated and said anode (claim 32). Dordi et al. further fail to teach said plated metal film forming unit is capable of raising and lowering said semiconductor substrate so as to correspond to respective operating conditions (claim 33). Nor do Dordi et al. (1) disclose said plated film forming unit is capable sealing said peripheral edge portion of said surface to be plated of said semiconductor wafer in an watertight manner (claim 34) or a pure water supply nozzle capable of simultaneously cleaning said semiconductor substrate and said cathode (claim 35).

84. Dordi et al. (2) disclose an plated film forming unit comprising: a substrate holding portion (Figure 4, 204; paragraph 38) for holding said semiconductor substrate such that a surface to be plated faces upward, an anode (230; paragraph 38) disposed above a surface to be plated, a cathode electrode (210; paragraph 38) for passing an electric current in contact with said substrate, and performs plating using a

Art Unit: 1763

plating liquid in a space formed between said surface to be plated and said anode. Dordi et al. teach said plated metal film forming unit is capable of raising and lowering (paragraph 75) said semiconductor substrate so as to correspond to respective operating conditions. Dordi et al. (1) disclose said plated film forming unit is capable sealing said peripheral edge portion of said surface to be plated (paragraph 59) of said semiconductor wafer in an watertight manner or a pure water supply nozzle capable of simultaneously cleaning said semiconductor substrate and said cathode. The plated film forming unit is constructed as described for the purpose of constructing a reliable and fast electroplating apparatus capable of delivering uniform power distribution to a substrate surface and capable of providing uniform deposition on a substrate surface (paragraph 13).

85. It would have been obvious to one of ordinary skill in the art at the time the Applicants's invention was made to have provided a plated film forming unit as described above in Dordi et al. (1) in order to construct a reliable and fast electroplating apparatus capable of delivering uniform power distribution to a substrate surface and capable of providing uniform deposition on a substrate surface as taught by Dordi et al. (2).

86. Examiner notes that with respect to the recitations drawn to properties of the processing fluid (e.g. plating liquid impregnated material comprising a water retaining material), the courts have ruled that expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim. Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969).

**87. Claims 37-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,267,853 to Dordi et al. (1) in view of U.S. Patent No. 6,309,981 to Mayer et al. and U.S. Patent Publication No. 2002/0157960 A1 to Dordi et al. (2).**

88. Dordi et al. (1) disclose the invention substantially as claimed in Figure 3 and comprising: a semiconductor substrate processing apparatus, comprising: a carry-in and carry-out section (210; column 5, rows 20) for carrying in and carrying out a semiconductor substrate having a surface on which a circuit is formed, the apparatus is capable of carrying in and out in a dry state by using spin/rinse/dry station



Art Unit: 1763

(212; column 5, row 24); a plated metal film forming unit (240; column 5, rows 41-46) for forming a plated metal film on said semiconductor substrate which has been carried in;; and a transport mechanism (216) for transporting said semiconductor substrate between said units.

89. However, Dordi et al. (1) fail to disclose the apparatus comprising a polishing unit for polishing at least part of said plated metal film on said semiconductor substrate.

90. Mayer et al. disclose using a polishing process after a plated metal film forming process and an edge bevel removal process in a semiconductor manufacturing process for the purpose of planarizing a substrate for further processing (column 5, rows 56-61).

91. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided a polishing apparatus for use after plating and edge bevel removal processes in Dordi et al. (1) in order to planarize a substrate for further processing as taught by Mayer.

92. Dordi et al. (1) and Mayer et al. disclose the invention substantially as claimed.

93. However, Dordi et al. (1) and Mayer et al. fail to teach comprises a substrate holding portion for holding said semiconductor substrate such that a surface to be plated faces upward, an anode disposed above a surface to be plated, a cathode electrode for passing an electric current in contact with said substrate, and performs plating using a plating liquid in a space formed between said surface to be plated and said anode (claim 37). Dordi et al. further fail to teach said plated metal film forming unit is capable of raising and lowering said semiconductor substrate so as to correspond to respective operating conditions (claim 38). Nor do Dordi et al. (1) disclose said plated film forming unit is capable sealing said peripheral edge portion of said surface to be plated of said semiconductor wafer in an watertight manner and formed between said surface to be plated an said anode (claims 39 and 42) or a pure water supply nozzle capable of simultaneously cleaning said semiconductor substrate and said cathode (claim 41).

94. Dordi et al. (2) disclose an plated film forming unit comprising: a substrate holding portion (Figure 4, 204; paragraph 38) for holding said semiconductor substrate such that a surface to be plated faces upward, an anode (230; paragraph 38) disposed above a surface to be plated, a cathode electrode (210; paragraph 38) for passing an electric current in contact with said substrate, and performs plating using a plating liquid in a space formed between said surface to be plated and said anode. Dordi et al. teach said

Art Unit: 1763

plated metal film forming unit is capable of raising and lowering (paragraph 75) said semiconductor substrate so as to correspond to respective operating conditions. Dordi et al. (1) disclose said plated film forming unit is capable sealing said peripheral edge portion of said surface to be plated (paragraph 59) of said semiconductor wafer in an watertight manner or a pure water supply nozzle capable of simultaneously cleaning said semiconductor substrate and said cathode. The plated film forming unit is constructed as described for the purpose of constructing a reliable and fast electroplating apparatus capable of delivering uniform power distribution to a substrate surface and capable of providing uniform deposition on a substrate surface (paragraph 13).

95. It would have been obvious to one of ordinary skill in the art at the time the Applicants's invention was made to have provided a plated film forming unit as described above in Dordi et al. (1) and Mayer et al. in order to construct a reliable and fast electroplating apparatus capable of delivering uniform power distribution to a substrate surface and capable of providing uniform deposition on a substrate surface as taught by Dordi et al. (2).

96. Examiner notes that with respect to the recitations drawn to properties of the processing fluid (e.g. plating liquid impregnated material comprising a water retaining material), the courts have ruled that expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim. Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969).

97. **Claims 63-64 and 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,267,853 to Dordi et al. (1) in view of U.S. Patent No. 5,310,410 to Begin et al**

98. Dordi et al. (1) disclose a semiconductor substrate processing apparatus substantially as claimed in Figure 3, comprising: a carry-in and carry-out section (210; column 5, rows 20) for carrying in and carrying out a semiconductor substrate having a surface on which a circuit is formed, the apparatus is capable of carrying in and out in a dry state by using spin/rinse/dry station (212; column 5, row 24); a plated metal film forming unit (240; column 5, rows 41-46) for forming a plated metal film on said semiconductor substrate which has been carried in; an annealing unit (211; column 5, row 20) for

Art Unit: 1763

annealing said semiconductor substrate; and a transport mechanism (216) for transporting said semiconductor substrate between said units. The processing apparatus of Dordi et al. (1) may further comprise a cleaning unit for cleaning said semiconductor substrate (one of modules 238; column 9, rows 1-6 and column 19, rows 5-10); and a liquid supply equipment (220; column 20, rows 51-64) having a plating liquid tank .

99. However, Dordi et al. (1) fail to teach the apparatus may further comprise a film thickness measuring instrument and/or a detection sensor for measuring and/or detecting a film thickness of a film and/or surface state of a film formed on said semiconductor substrate.

100. Begin et al. teach that an inspection unit may be included as part of a cluster apparatus for the purpose of determining whether a substrate or a portion of the apparatus is defective (column 4, rows 48-54).

101. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided an inspection unit in Dordi et al. (1) in order to determine whether a substrate or a portion of the apparatus is defective as taught by Begin et al.

### ***Conclusion***

102. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. USP 5,769,952 discloses a multi-chamber apparatus comprising both reduced pressure treatment units and normal pressure treatment units.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Karla Moore whose telephone number is 571.272.1440. The examiner can normally be reached on Monday-Friday, 8:30am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory Mills can be reached on 571.272.1439. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 1763

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'K Moore', is positioned above the typed name.

Karla Moore  
Art Unit 1763  
18 March 2005